

FIG. 1

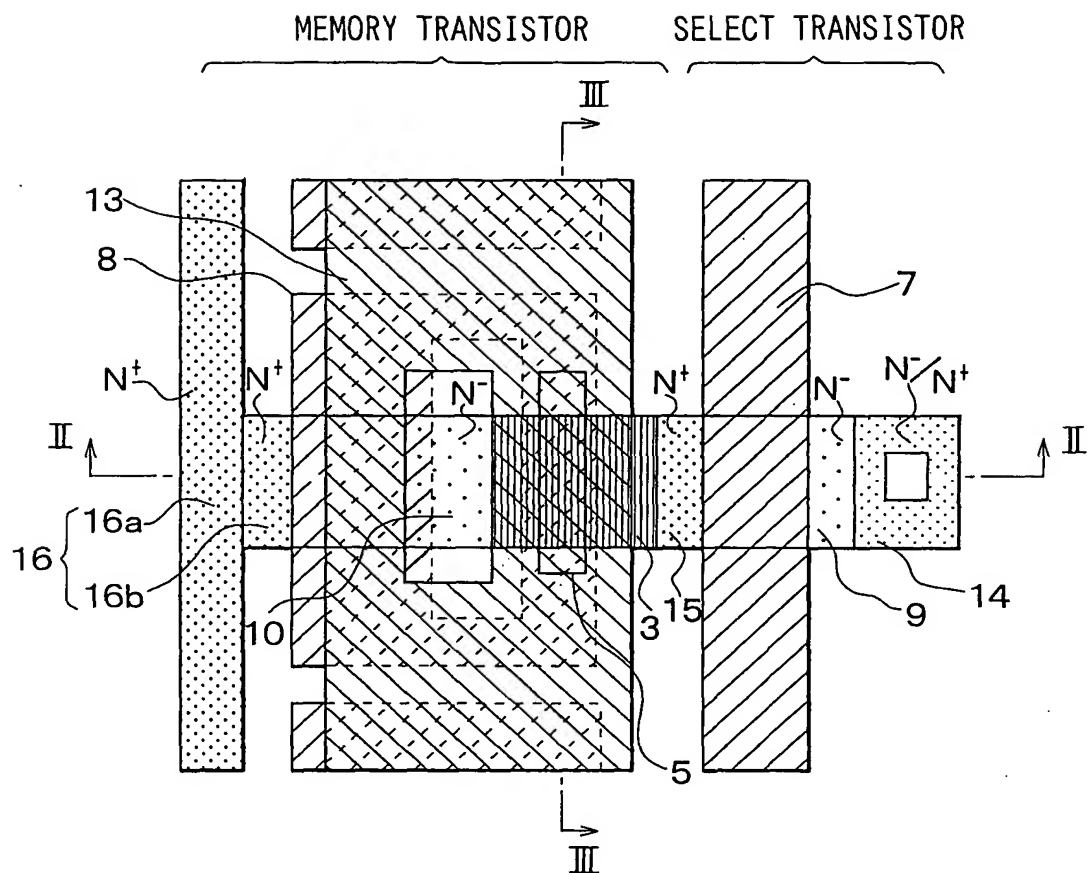


FIG. 2

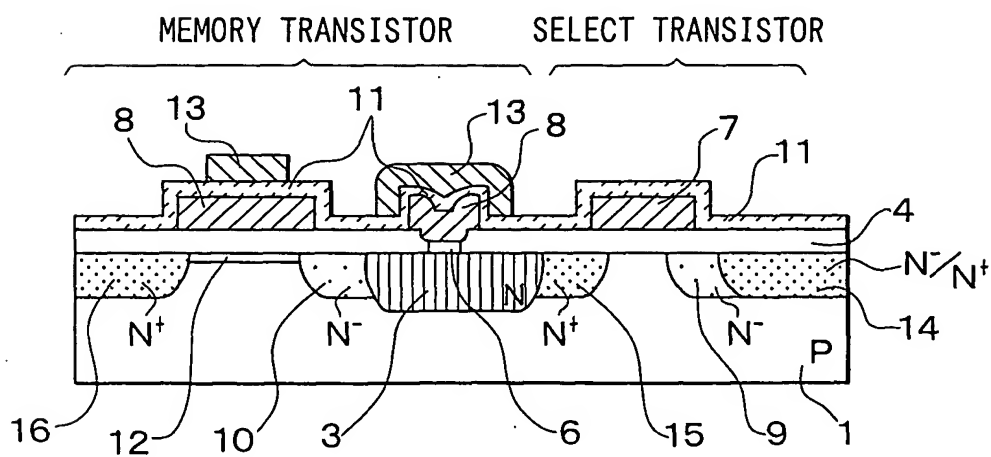


FIG. 3

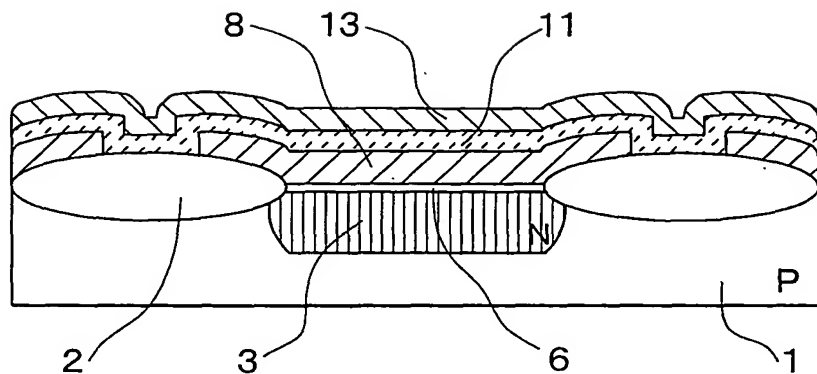


FIG. 4A

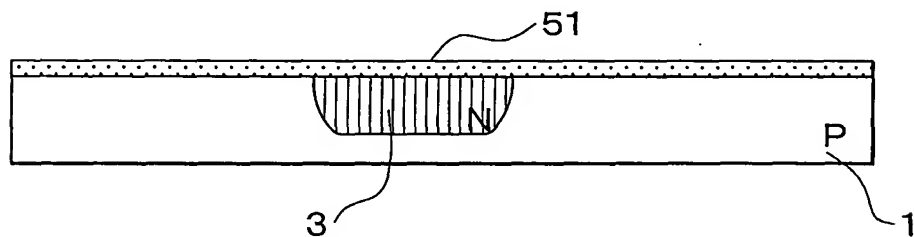


FIG. 4B

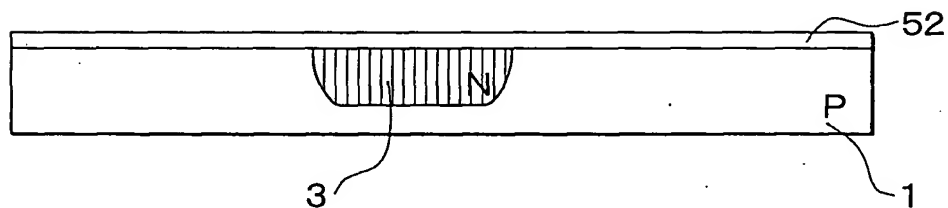


FIG. 4C

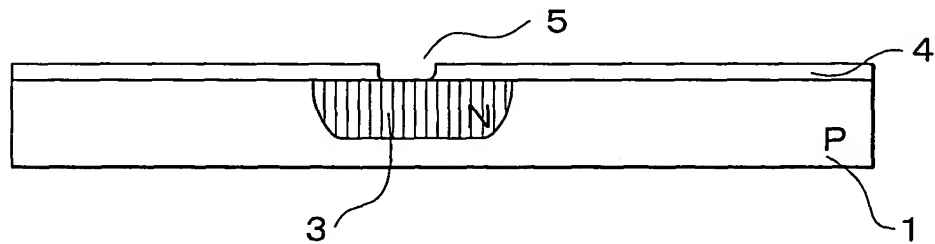


FIG. 4D

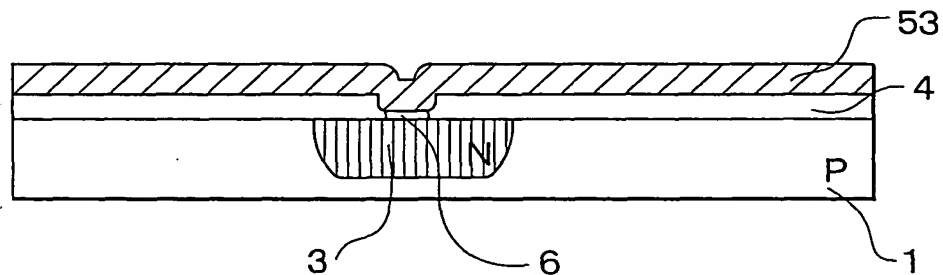


FIG. 5A

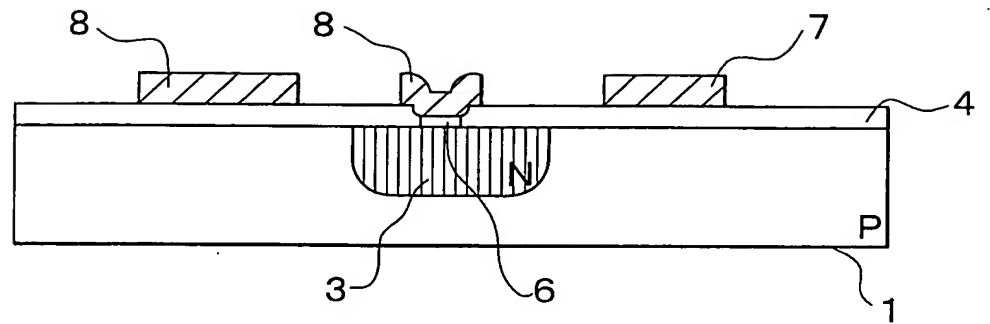


FIG. 5B

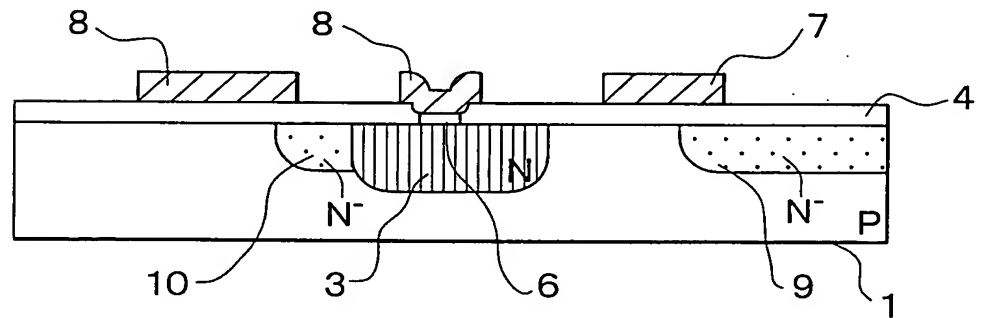


FIG. 5C

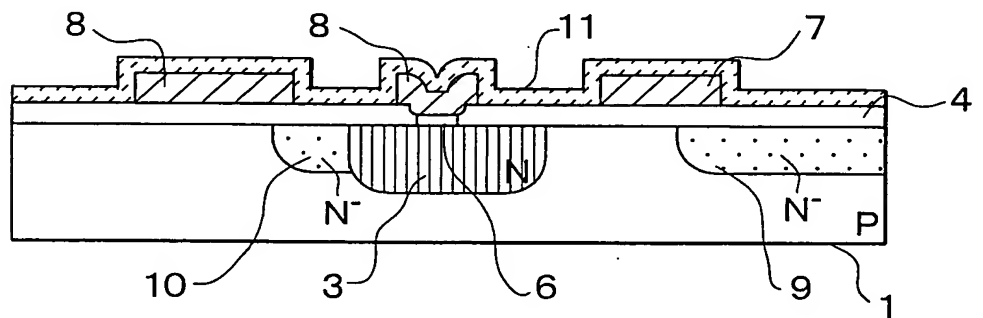
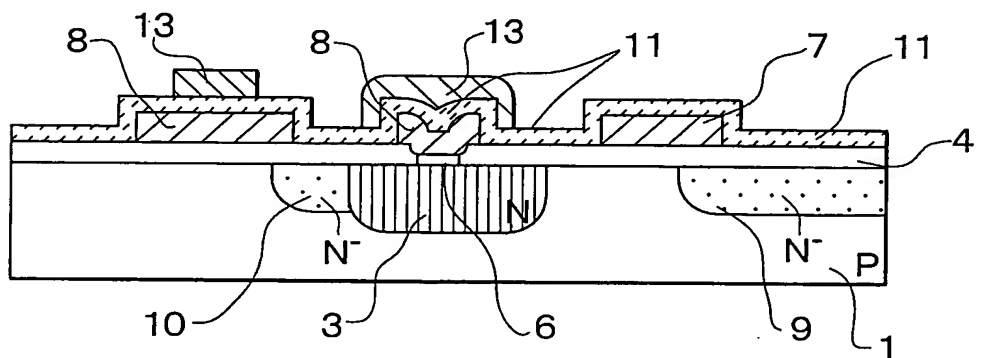


FIG. 6A



A cross-sectional view of a semiconductor device. The device consists of a substrate 1 with a P-type region 14. On the substrate, there are several layers and regions: a layer 4, a layer 11, and a layer 7. A central channel region 3 is defined by a gate stack 13 and a gate 11. The channel region 3 is surrounded by N⁺ regions 10 and N⁻ regions 9. A side region 15 is also shown. Other labels include 8, 13, 16, and 10.

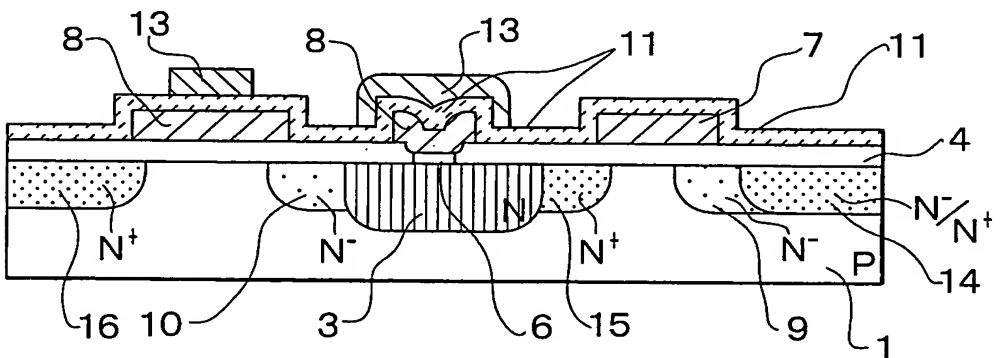


FIG. 7A

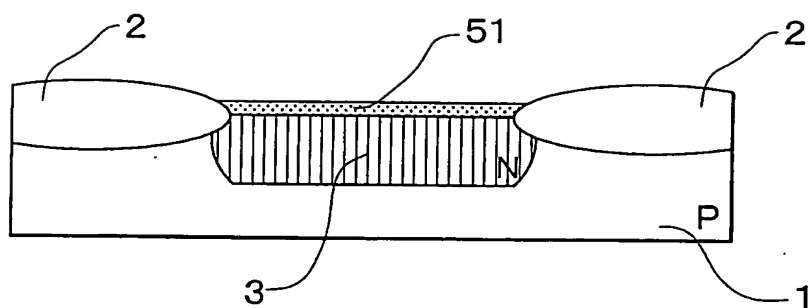


FIG. 7B

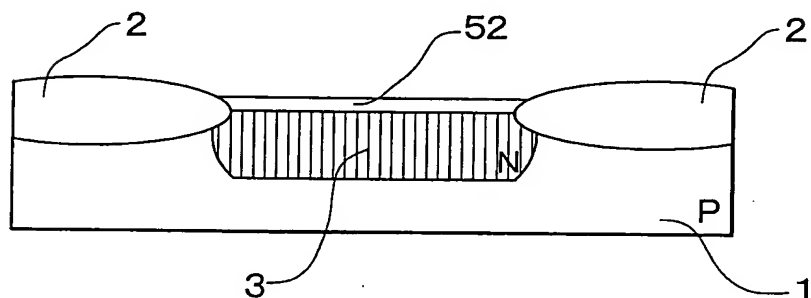


FIG. 7C

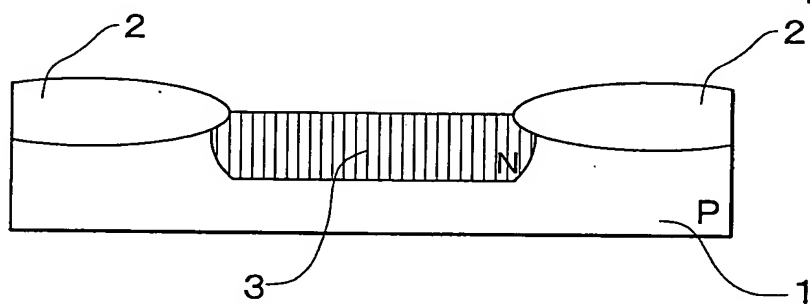


FIG. 7D

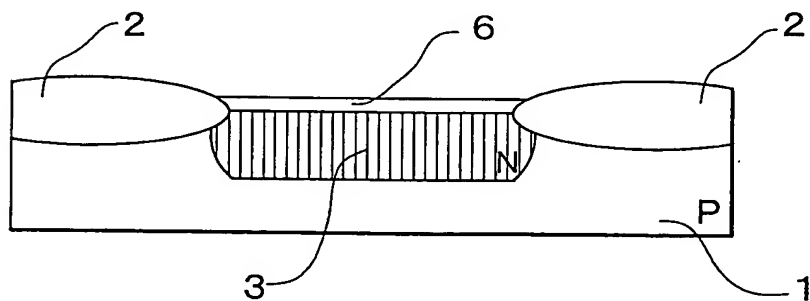


FIG. 8A

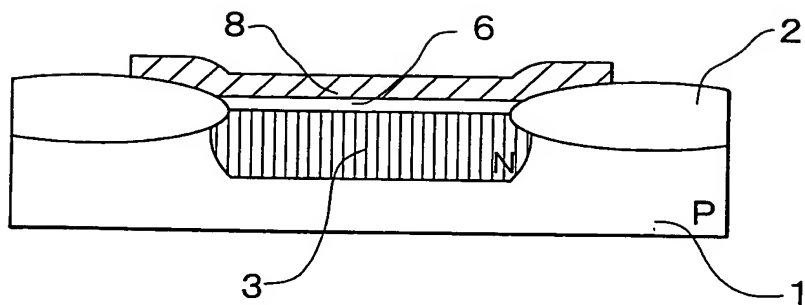


FIG. 8B

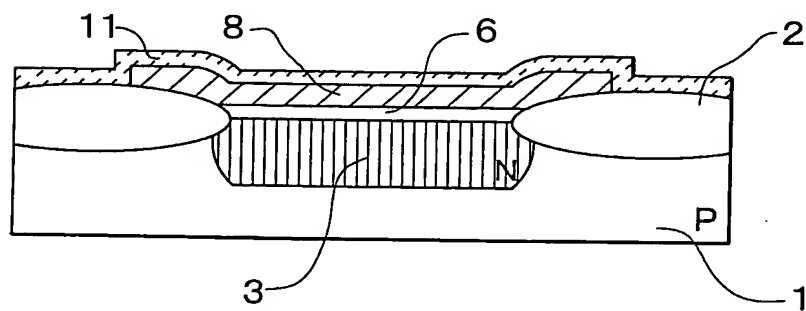


FIG. 8C

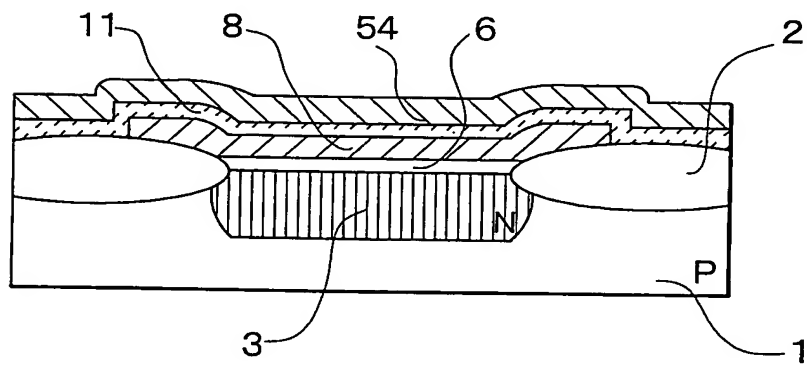


FIG. 8D

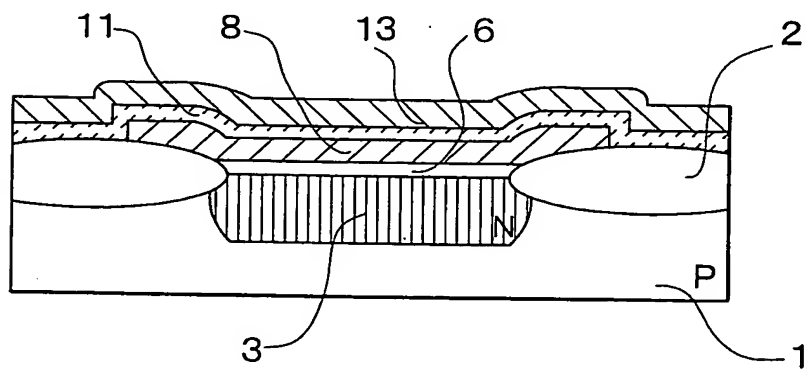


FIG. 9

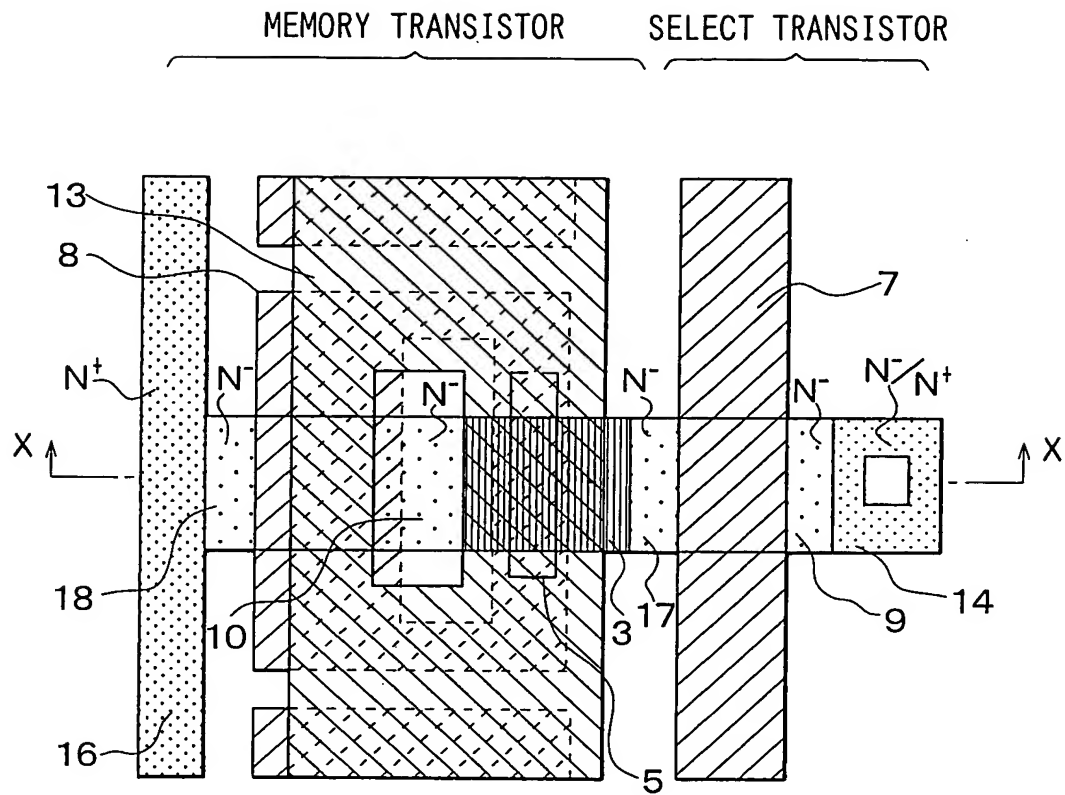


FIG. 10

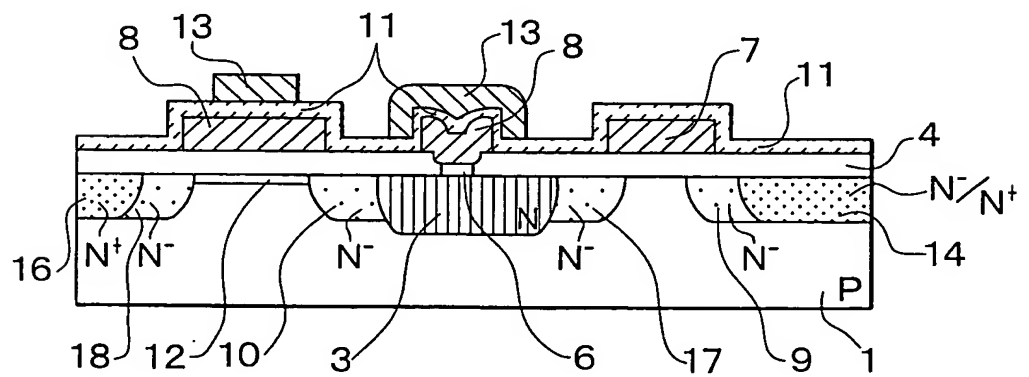


FIG. 11A

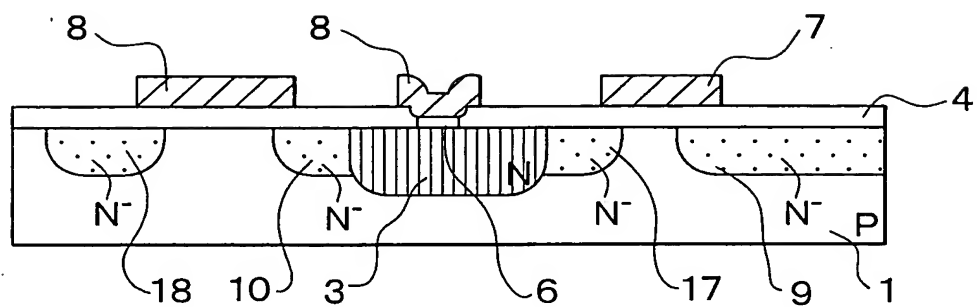


FIG. 11B

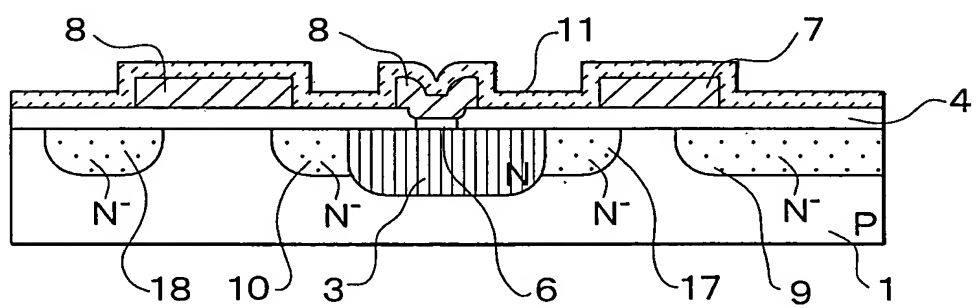


FIG. 12A

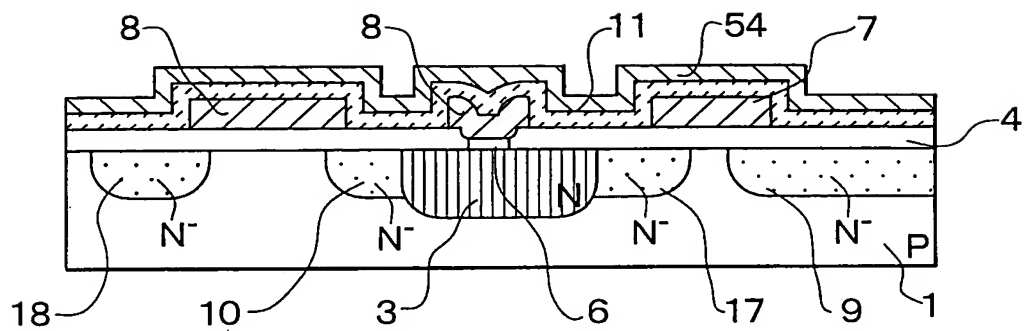


FIG. 12B

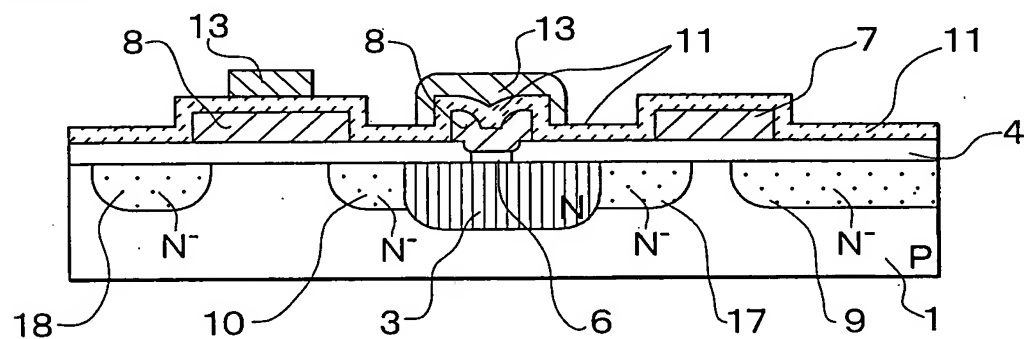


FIG. 12C

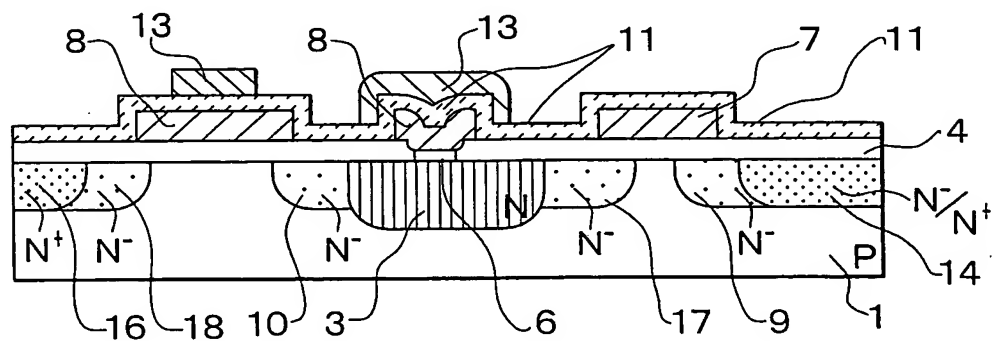


FIG. 13

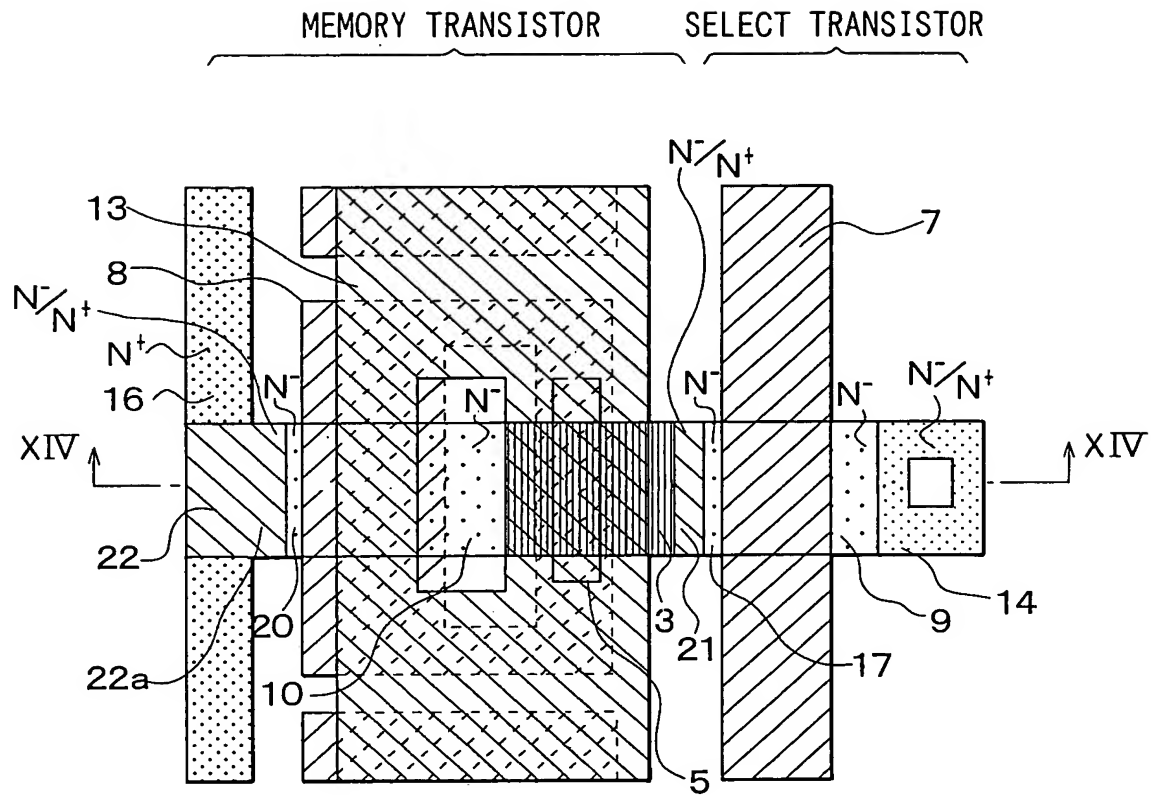


FIG. 14

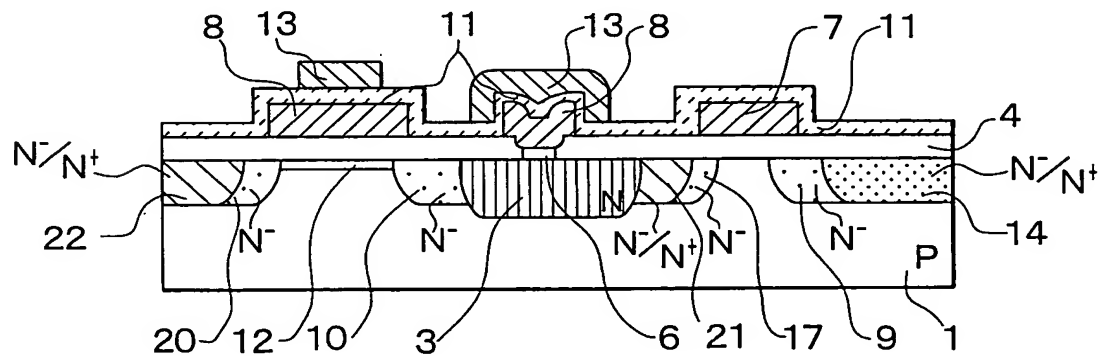


FIG. 15A

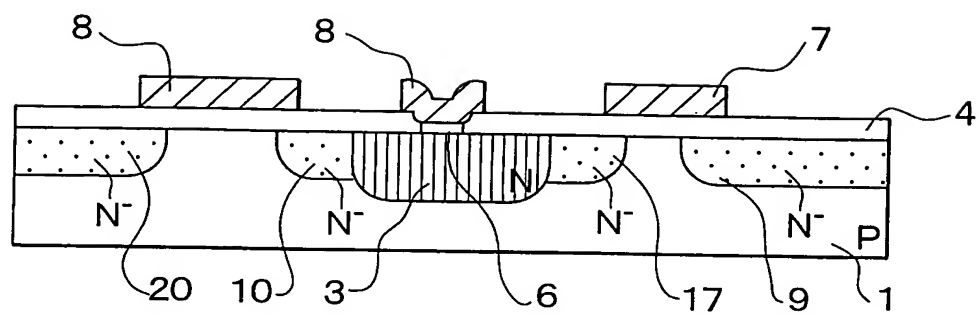
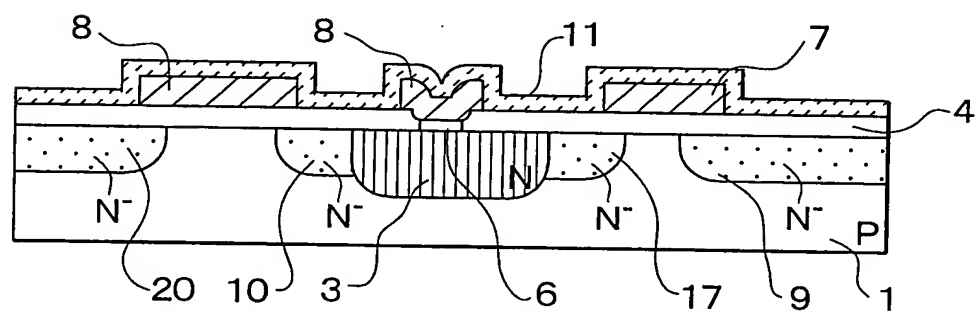


FIG. 15B



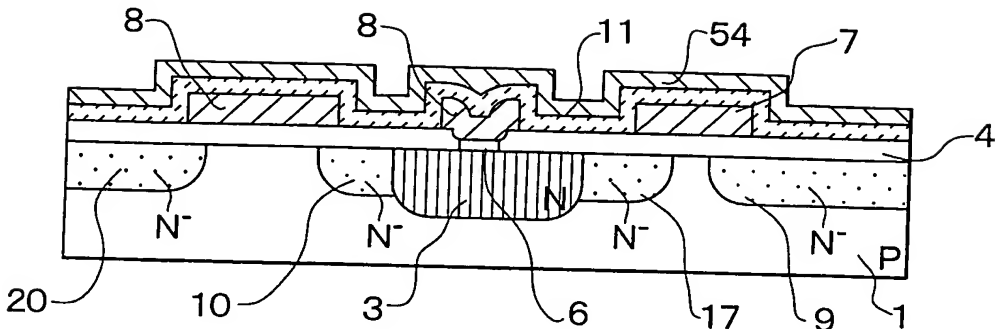


FIG. 16B

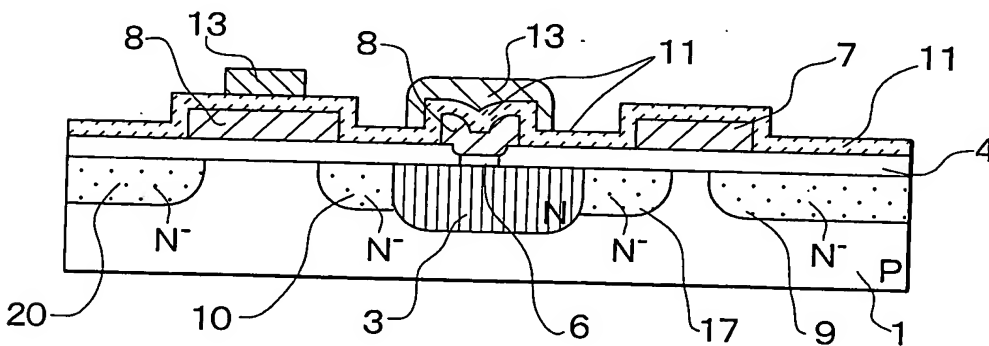


FIG. 16C

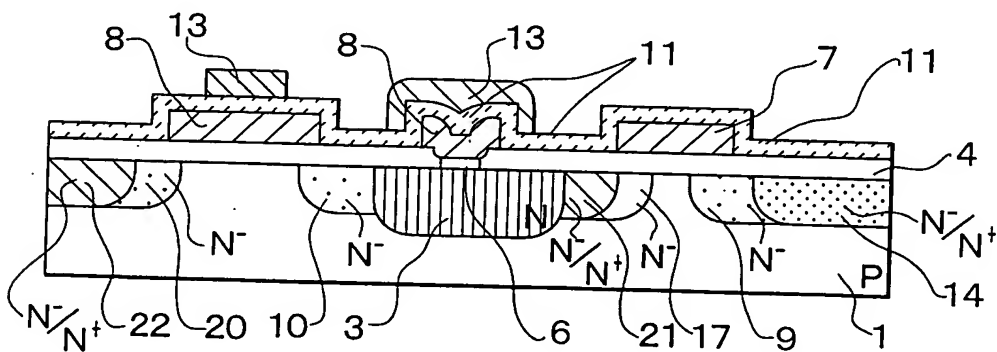


FIG. 17

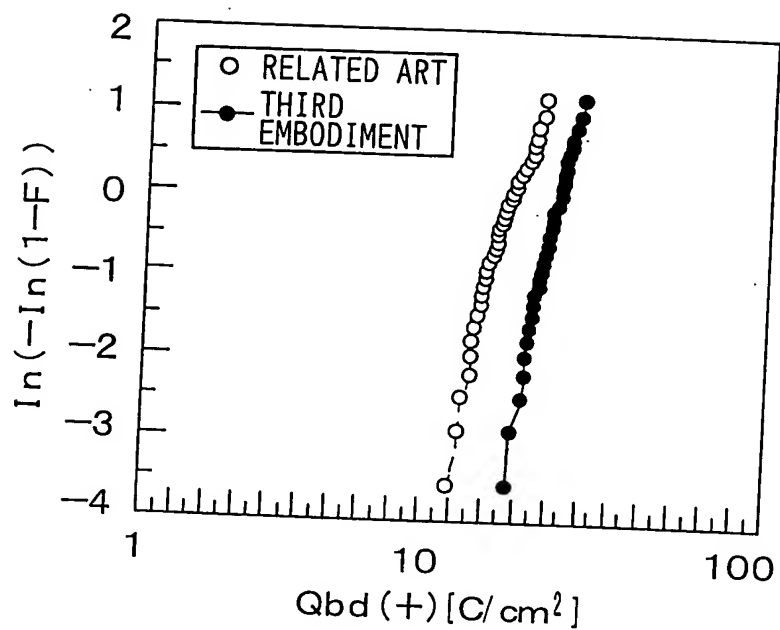


FIG. 18

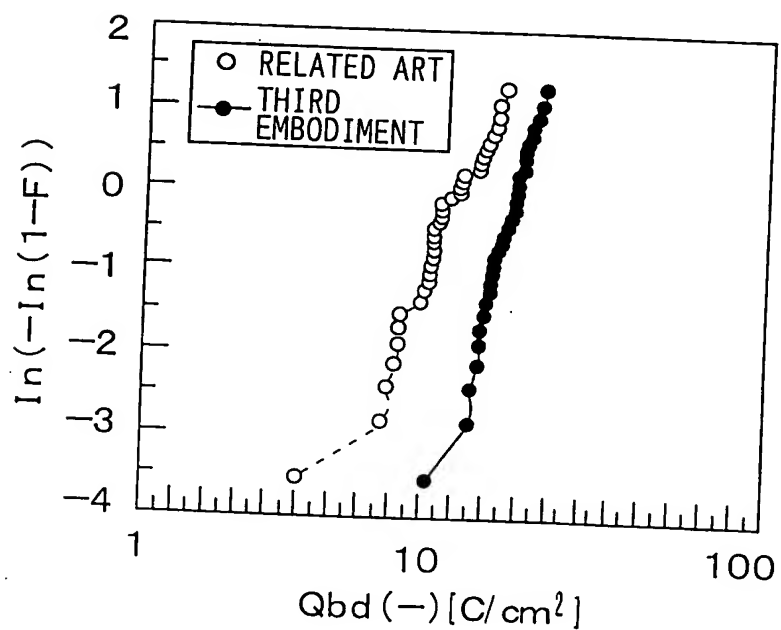


FIG. 19

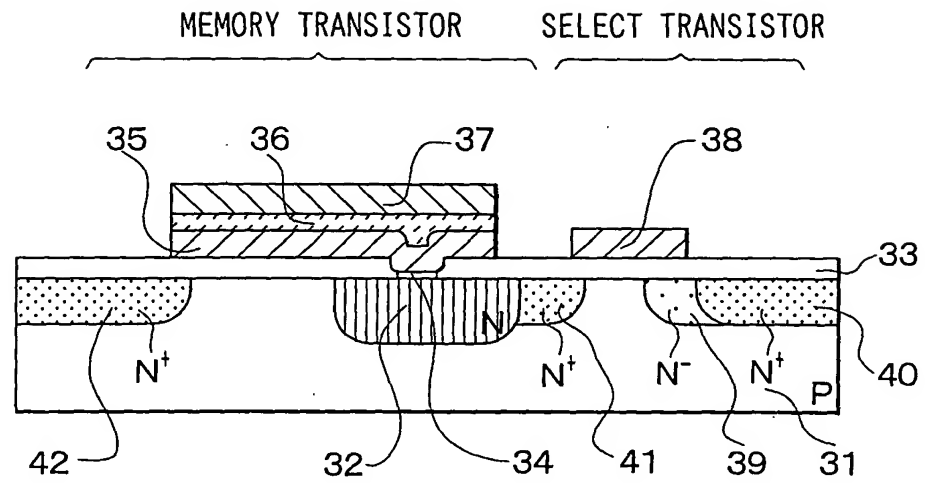


FIG. 20

